WP4 – Description of Work

Objectives
Improve advanced CMOS device yield compare to state-of-the-art baselines by developing and qualifying a computing system which will serve the semiconductor manufacturers to tie together process, metrology and design data by improving both process defects analysis and tools health monitoring performances.
Develop methodologies that can be extended to other applications from the data-science point of view related to smart sampling, feature engineering requirements, and recommended machine learning approaches.

Planned work
To accomplish the main objective, WP4 will consist of multiple tasks distributed around two main tasks covering wafer processing for active device and interconnect, and package-related processing. Both tasks will cover wafer, or die level measurements as required. The work package is organized into the following tasks and sub-tasks (tasks 4.1.1.1, 4.1.1.2 and 4.2.1 are those in which POLITO is involved):

4.1. Predictive Yield for Semiconductor and Automotive manufacturing
4.1.1 Develop and benchmark smart algorithms for process defectivity predictions
4.1.1.1. Feature engineering for wafer, packaging, and automotive manufacturing processes
4.1.1.2. Defining sampling strategy for training and predicting the behaviour of subsequent wafer, packaging and automotive body and assembly shop floor critical areas datasets undergoing the same nominal operation conditions.
4.1.2 Develop and benchmark next generation process and diagnostic control for yield, and productivity enhancements.
4.2 Predictive tools performance and availability for Semiconductor and Automotive manufacturing
4.2.1 Develop Predictive tools performance and availability
4.2.2 Develop and benchmark smart algorithms for process variation flag raising
4.3 Computing platforms and smart sensors for fast data acquisition and analytics
4.3.1 Computing platform for fast data acquisition and analytics
4.3.2 Fast computing platform of Twin Images recognition with Neural Algorithm
4.3.3 Smart Imager for fast data acquisition incorporating on-chip realisation of Neural network, predictive sampling and sensor fusion

Task 4.1.1.1. **Feature engineering for wafer, packaging, and automotive manufacturing processes**

Partners: MENT, AMIL, BJV, GF, ICOS, IMEC, NOVA, IPPON, FCA-ITALY, COMAU, ST-I, POLITO, TOWER

Objective: Characterize machine learning input vector to capture the effects of interest.

Description: Most of the existing semiconductor manufacturing tools focus on litho-hotspots and mainly only one design layer is being used for characterization., in the same way in the packaging and automotive manufacturing processes the goal of this work is to determine the way to apply domain knowledge to adequately characterize the input vector to capture the effects of interest (Feature Engineering).

Contribution of automotive partners: Automotive partners will work on feature engineering using both OEM and Technology Provider knowledge (product design, process design and simulation, data collected by both IIoT layer and production information systems), mainly with reference to data and events related to quality, maintenance, logistics to discover dependencies / relationships with manufacturing processes and product configurations. CNR will develop the formal apparatus for the integration of simulation and black (and grey)-box models. Some advanced concepts in the field of the Machine Learning (e.g. the quantum versions of the algorithms) will be also explored and theoretically benchmarked. These numerical tools will be applied, calibrated and validated in the WP5 in the reference industrial environment. POLITO will evaluate solutions for the filtering of input features with the objective of reducing the complexity of their extraction.

Task 4.1.1.2: Defining sampling strategy for training and predicting the behaviour of subsequent wafer, packaging, and automotive manufacturing process datasets undergoing the same nominal operation conditions.

Partners: MENT, AMIL, BJV, IPPON, NOVA, GF, ICOS, IMEC, TUE, UPB, FCA-ITALY, COMAU, POLITO, ST-I, CNR, TOWER, LETI, MEL, SEMIL, AVL, VIF

Objective: Determine the sampling strategies to continuously improving the quality of the machine learning models.

Description: In semiconductor manufacturing the cost of measuring every chip in every wafer, in every lot is not practical. This task should determine the sampling strategies to continuously improving the quality of the machine learning models, in particular machine learning approaches that can learn from few examples.
In automotive manufacturing processes, there is a multitude of individual and interdependent measurements which cannot be all captured with the same temporal resolution, in this task we will determine the sampling strategy required to design, calibrate and augment tool specific models.
In addition, most manufacturing organizations recognize that there can be changes in the process that may (or may not) cause changes in the nominal response of a specific electronic product. By collecting the second dataset under the same nominal conditions but at a different time, we believe that we can address the issue of predictive maintenance, in which by combining the monitoring of different processes operating at their nominal conditions, we detect process drift.

Contribution of automotive partners: Will provide sampling strategies related both to Product Quality and Predictive Maintenance based on the learning performed in task 4.1.1.1.

Task 4.2.1: Develop Predictive tools performance and availability

Partners: THERMO, MENT, AMIL, ICOS, IMEC, TUE, FCA-ITALY, COMAU, ST-I, CNR, POLITO, ST-C, ST-R, IMT, AMU, AVL, VIF

Objective: Using methods developed in task 4.1, develop predictive software tools in areas of tool performance, and tool’s health and availability.

Description: Algorithms and methodologies will be developed to monitor and optimize tool health and availability. Based on these, optimized, pro-active maintenance schedules can be derived and executed, while at the same time providing the state indicators (KPI’s) to higher level processes if needed. Due to tool drift and lack of tool matching, metrology tools give different results, and produce metrology mismatch which can erroneously characterize the wafer processes and the device structures. This metrology issue can be addressed once more systematic tool monitoring is in place.

Contribution of automotive partners: Based on methods and sampling techniques defined in 4.1.1 partners develop machine learning algorithms to highlight conditions impacting equipment control and pre-warn applications and process KPIs. POLITO will focus on a characterization of the algorithms in terms of their computational complexity/prediction accuracy trade-off with the objective of determining the most suitable one for a given computational platform (edge node). Based on the results above, FCA will design data and data science layers and related interfaces for data technologies to be put in place for applications development in WP5.